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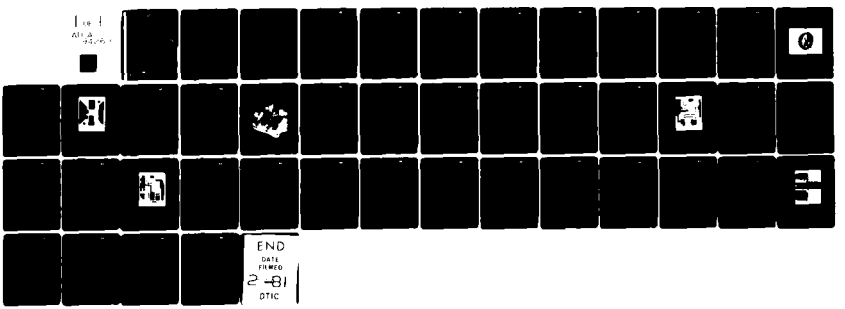

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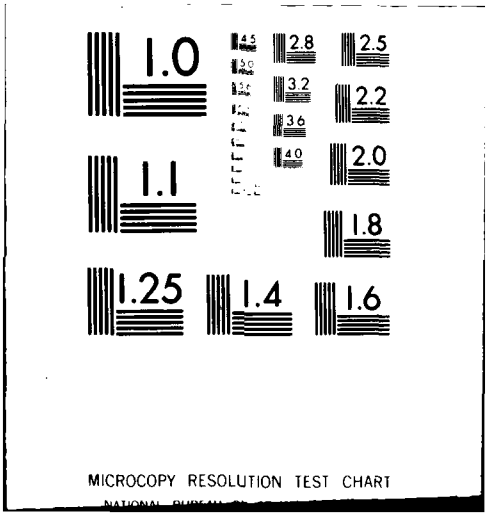
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MONOLITHIC GaAs SUPERHETERODYNE FRONT END

Interim Report for the period
August 15, 1978 through August 14, 1979

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This report describes the progress during the first phase of the development of a monolithic Gallium Arsenide Superheterodyne Front End for the 8GHz military satellite communications band. The integrated GaAs receiver chip is to be fabricated using the monolithic microwave integrated circuit (MMIC) approach. It will contain an RF preamplifier, an FET mixer, and an IF amplifier. A monolithic GaAs local oscillator will be developed under a separate program. This

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20. report describes the design and the fabrication of the three circuits to be integrated. Functional monolithic circuits have been fabricated and are being characterized at present. The IF amplifier has shown 8.0 ±1.5 db gain and 6.25 db maximum noise figure in the 500 - 1000 MHz frequency band. RF performance of the preamplifier and the mixer will be described in the next report.

FOREWORD

This report describes the progress under ONR Contract #N00014-78-C-0624 between August 15, 1978 and August 14, 1979. The goal of this program is to develop a superheterodyne receiver front end for the 8GHz military satellite communications band using the GaAs monolithic microwave integrated circuit (MMIC) approach. The work described herein was carried out at Rockwell International Electronic Research Center, P. O. Box 1085, Thousand Oaks, California.

The program manager and principal investigator is Dr. D. R. Ch'en. Other members of staff who have contributed to his program are: Drs. D. R. Decker, A. K. Gupta, J. A. Higgins, and W. Petersen. Mr. M. N. Yoder of the Office of Naval Research is the technical monitor of this program.

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CHAPTER 1

Introduction

This report describes the progress under ONR Contract #N00014-78-C-0624 between August 15, 1978 and August 14, 1979. The goal of this program is to develop a monolithic gallium arsenide (GaAs) superheterodyne receiver front end for the 8 GHz military satellite communications band using the monolithic microwave integrated circuit (MMIC) approach. This new technological approach to microwave circuitry is based on the unique capabilities of GaAs material in conjunction with ion implantation for precise control of active region doping. The insulating properties of GaAs semi-insulating substrates with resistivities as high as 10^9 Ω-cm allow monolithic integration of active devices, bias networks, and microwave circuitry on a single GaAs chip. Ion implantation doping technology facilitates control of multiple doping densities for optimization of active devices and also permits fabrication of highly planar circuits to achieve superior yields. This monolithic technology is expected to yield circuits with the following attributes:

(1) small size,
(2) lightweight,
(3) low cost,
(4) reproducible performance,
(5) broad bandwidth capability, and
(6) multi-functional performance

The integrated GaAs receiver chip that will be fabricated in this program is to contain an RF preamplifier, an FET mixer, and an IF amplifier. A monolithic GaAs local oscillator will be developed under a separate program. Receiver specifications are as follows:

Frequency band:	7.75 - 8.25 GHz
Maximum receiver noise figure:	3.9 dB
Minimum RF to IF gain:	30 dB

In order to realize this goal in an expedient manner, the approach is to first design, fabricate and characterize the three individual receiver components prior to the integration of the receiver chip. The initial component designs have been fabricated and circuit characterization is now underway. The IF amplifier has shown 8.0 ± 1.5 dB gain and 6.25 maximum noise figure in the 500-1000 MHz frequency band. The RF preamplifier and the FET mixer are currently being characterized.

This report is organized as follows. Chapter 2 contains a description of the design and the performance of the three circuits to be integrated. A discussion of the factors limiting the performance of these circuits is also given. The circuit fabrication technology is described in Chapter 3. Finally, in Chapter 4, a summary of the major program accomplishments is presented, and an outline of plans for the next period is described.

CHAPTER 2

Design and Performance of Functional Monolithic Circuits

Circuit design considerations and performance results of the IF amplifier are discussed in this chapter. A discussion of the 8 GHz preamplifier and mixer circuits is also presented. Characterization of these circuits is now underway, and the performance will be included in a later report. Figure 2.1 is a photograph of these three circuits on a U.S. dime.

2.1 IF Amplifier

2.1.1 Circuit Design

The IF amplifier was designed to be compact and to contain on chip biasing circuitry. The compact design was made possible by elimination of inductive matching elements, although it is likely that some form of tuning will be required when the amplifier is integrated with the mixer output circuitry for best gain and noise performance. The amplifier was designed using the COMPACT CAD program. The dual-gate FET was modeled using an equivalent circuit composed of single-gate FET equivalent circuits in the common source and common gate connection. A circuit diagram of the IF amplifier is shown in Fig. 2.2 and an SEM photograph of the circuit fabricated on GaAs is shown in Fig. 2.3.

Microstrip circuitry on a 0.635 mm thick semi-insulating GaAs substrate is the chosen transmission mode for this amplifier. RF grounding of the active devices is accomplished with top surface ground planes along each edge of the chip. At the IF frequencies, grounding inductance is quite acceptable with this approach. Input and output of the IF amplifier are via 50 Ω transmission lines which are isolated by metal-insulator-metal (MIM) coupling capacitors (10 to 20 pF). Bias lines are provided for each of the FET gates and for V_{dd}. All bias lines are bypassed by MIM capacitors of 7 to 12 pF in value. An interdigital coupling capacitor of value 0.6 pF is used to couple the output of the dual gate FET to the gate of the source follower output stage and simultaneously provide dc bias isolation. The high impedance at

Fig. 2.1 This photograph shows the RF preamplifier (left), the FET mixer (center), and the IF amplifier (right) on the face of a dime. The preamp and the mixer are each 2.5×2.5 mm^2 and the IF amplifier is approximately 2×2 mm^2 in size.

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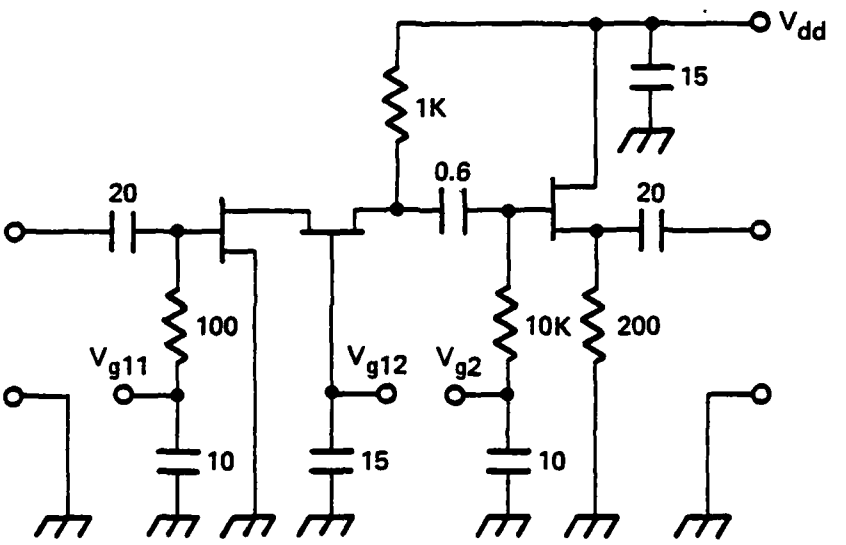


Fig. 2.2 IF amplifier schematic circuit.

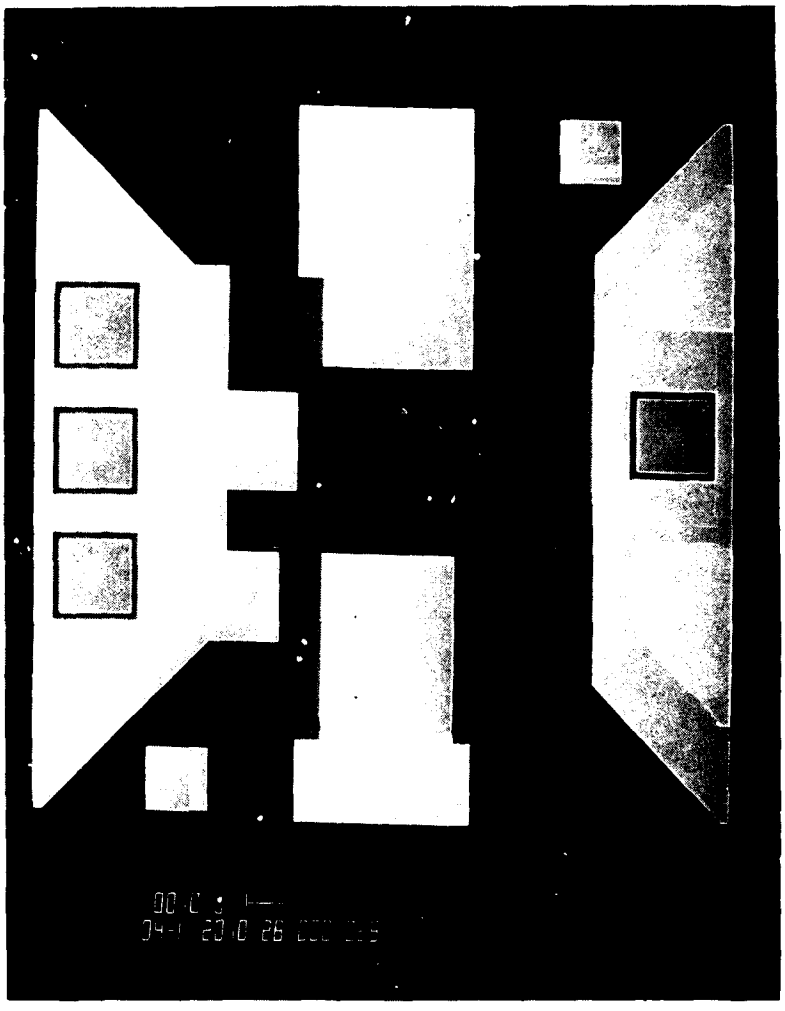


Fig. 2.3 SEM photograph of IF amplifier chip. Chip size is approximately 2×2 mm^2.

this point permits the usage of a relatively small coupling capacitor at low frequencies. However, any parasitic shunt capacitance to the ground plane will have a deleterious effect on amplifier performance.

Since the noise figure of the IF amplifier will be reduced by at least 20 dB of gain from the preceding preamplifier and mixer, the noise performance was not a primary design concern. The amplifier was designed to provide a nominal gain of 10 dB between 500 and 1000 MHz as shown in Fig. 2.4. The input match to 50 Ω is required for testing convenience only and is determined by a shunt 100 Ω resistor to ground to be about 2:1 VSWR. This resistor will not be necessary in the integrated version of the receiver front end. An excellent output match to 50 Ω is obtained with active matching by using an FET in the common drain connection. In this configuration, the output impedance is approximately equal to the inverse of the FET transconductance. Thus a transconductance of about 20 mS is appropriate for matching to a 50 Ω line. A 200 Ω shunt resistor is used at the output for biasing the source of the output transistor.

2.1.2 Test Results

Completed circuits are mounted into a microstrip test fixture as shown in the photograph of Fig. 2.5. The circuit is bonded between two alumina microstrip circuits which carry connections for input and output transmission lines and bias leads. In the frequency range of interest, this test fixture has been characterized to have less than 0.2 dB insertion loss with VSWR less than 1.07:1 at input and output (>30 dB return loss). The test fixture is connected to the measurement system using SMA type connectors. Bias is applied at the four screw terminals which are additionally bypassed with 1 μF ceramic capacitors.

The monolithic IF amplifier has been characterized for gain, isolation, and input and output match across the band from 500 to 1500 MHz. The measured gain is compared to the predicted gain in Fig. 2.6. As may be seen from the figure, the measured gain is about 3 dB below the predicted gain at 500 MHz and about 4 dB below the predicted curve at 1000 MHz. The lower gain

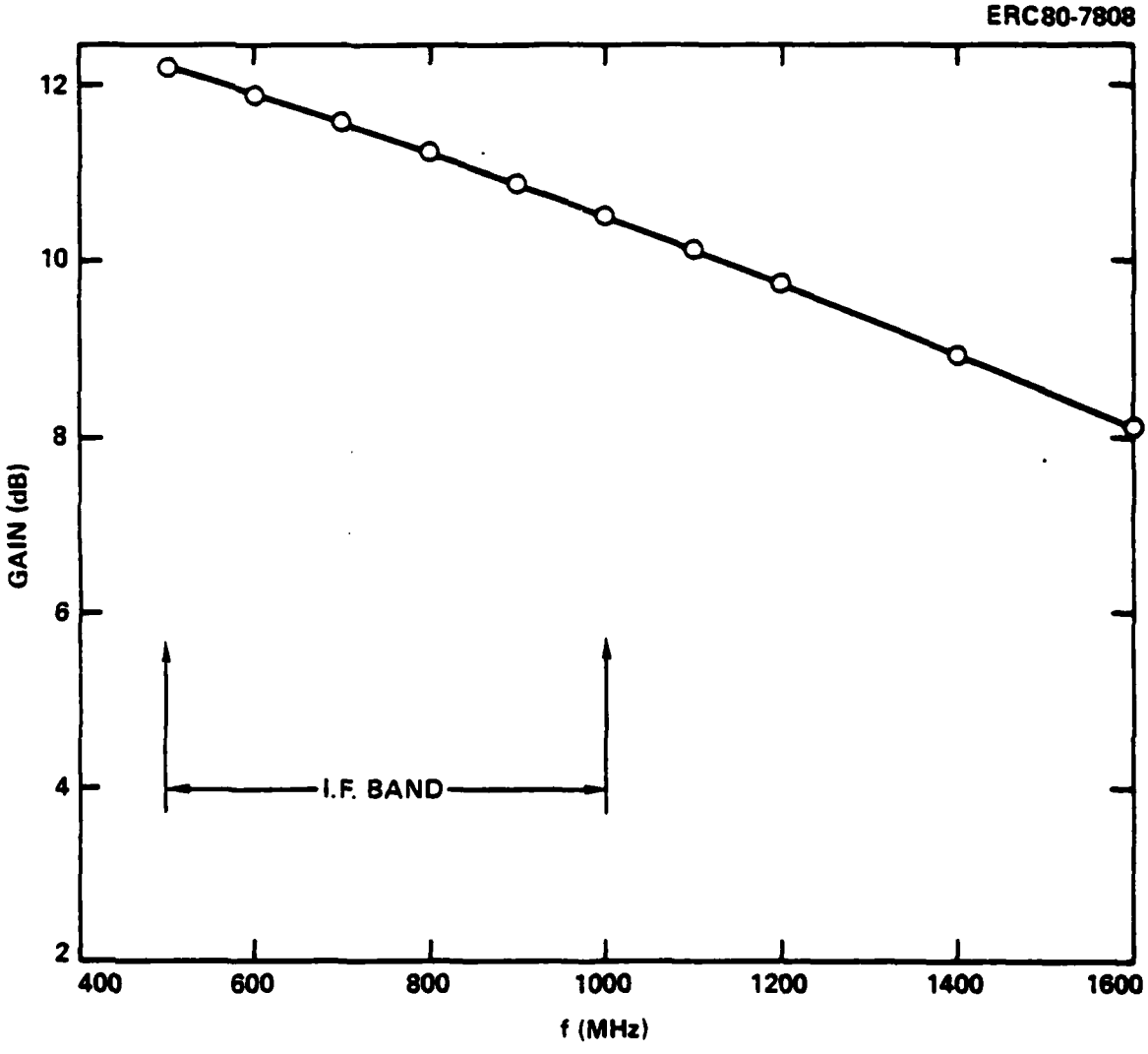


Fig. 2.4 Calculated gain of IF amplifier.

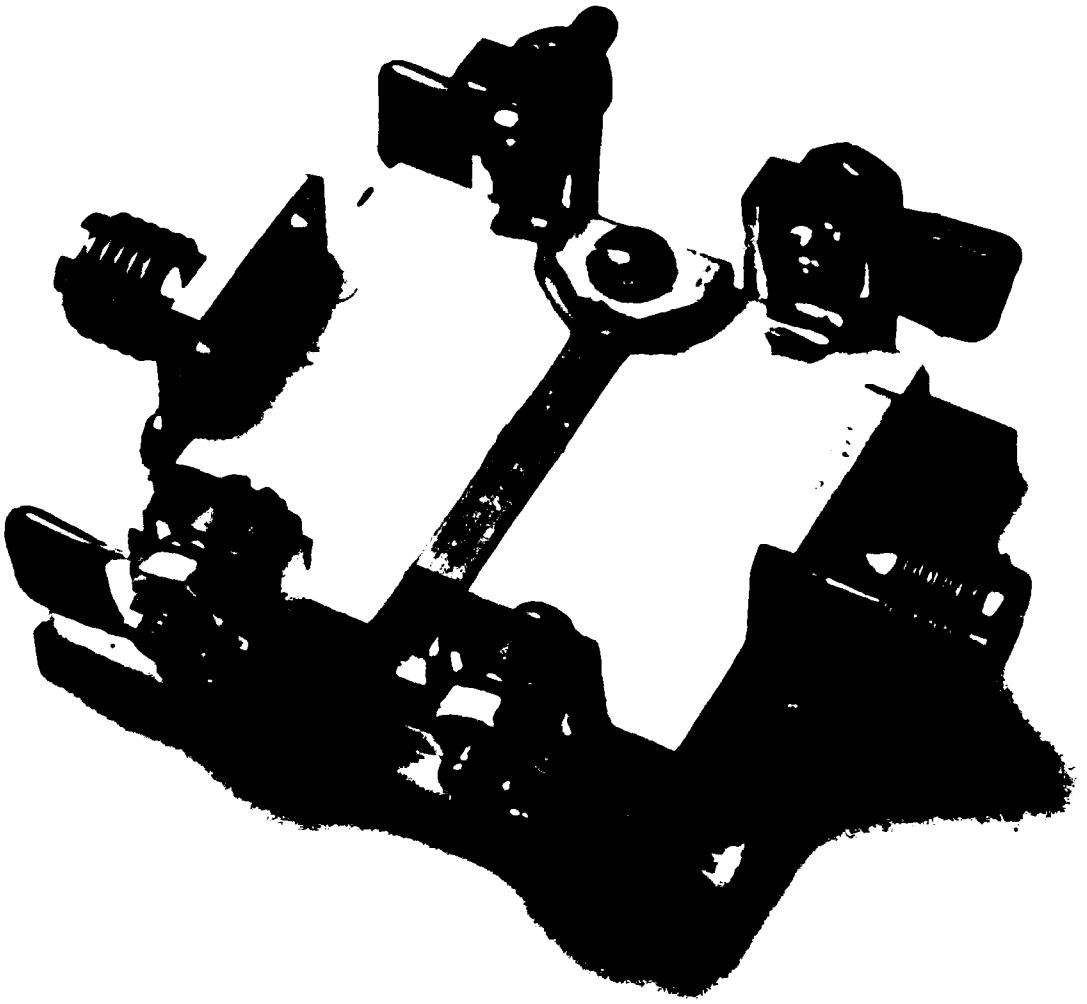


Fig. 2.5 Photograph of circuit mounted in test fixture.

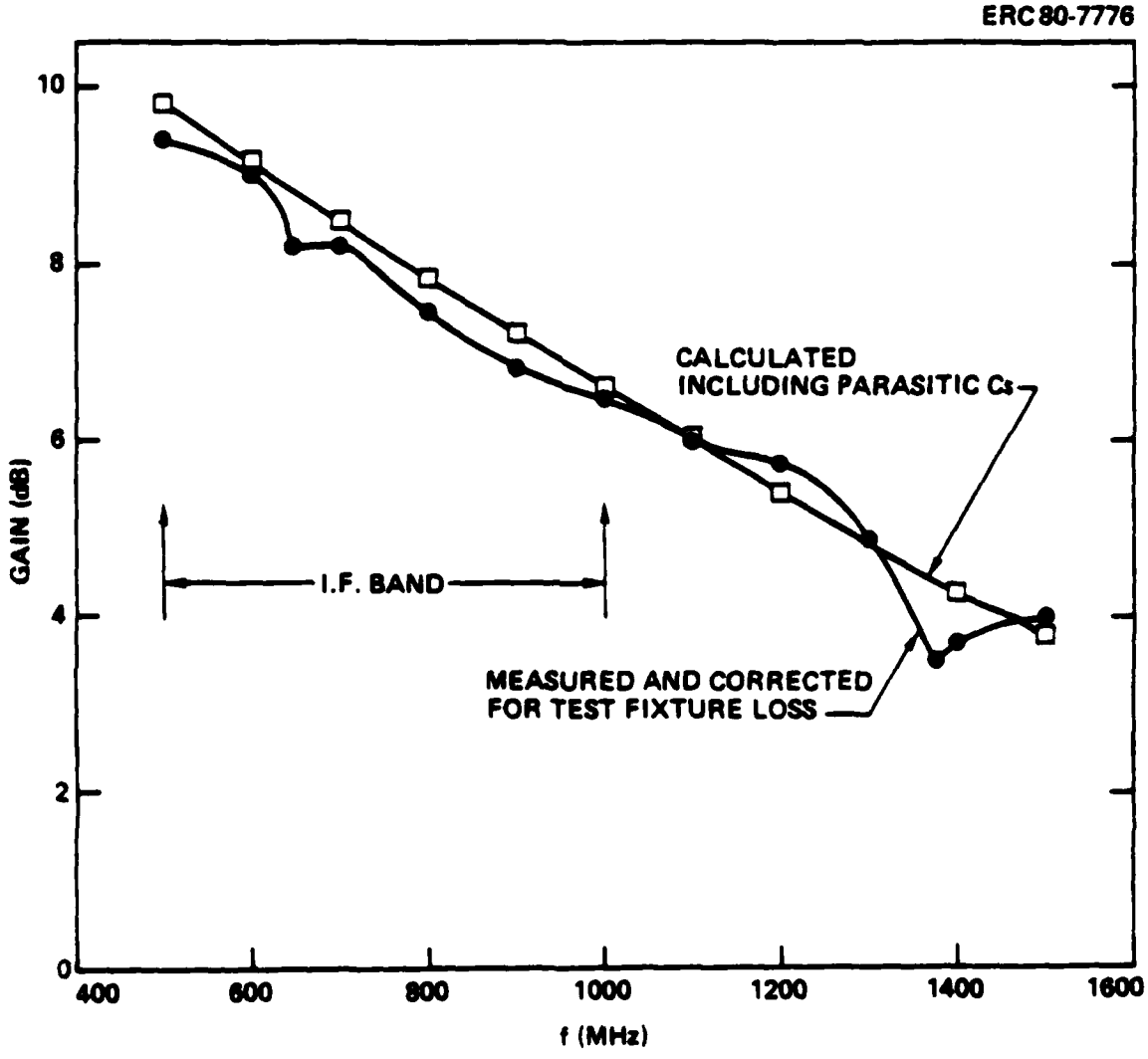


Fig. 2.6 Measured gain of IF amplifier.

and increased gain slope can be attributed to parasitic capacitances associated with the relatively large size of the interdigital coupling capacitor which were not included in the initial circuit design. The calculated gain including these additional parasitics is seen to closely predict the observed performance. These parasitics are being minimized through reconfiguration in a second version of this circuit.

The input and output return loss measured for the IF amplifier are shown in Fig. 2.7. The input VSWR is determined primarily by the 100 Ω shunt resistor and 7.5 pF bypass and 20 pF isolation capacitors in the input network. The input return loss is about 3 dB smaller than predicted which may be attributed to a reduced value for the bypass capacitor from 10 pF to 7.5 pF in the mask layout. Since, as previously mentioned, the input match is not a primary concern for this amplifier this result is satisfactory. The output match obtained using the source follower configuration is very good across the band from 500 to 1000 MHz as seen in Fig. 2.7. Output return loss is better than about 15 dB between 800 and 1500 MHz (except at 1100 MHz) dropping to about 10 dB at 500 MHz. The reduction of output return loss near the low end of the band may again be attributed to somewhat low values of bypass capacitors.

Noise figure of the IF amplifier was tested across the 500 to 1000 MHz band. The measured noise figure was 8 dB across the band which, when corrected for the noise of the 100 Ω shunt resistor which will not be present in the final configuration, gives an amplifier noise figure of about 6.25 dB. Noise tuning of the interstage matching could be used to reduce these values when this amplifier is integrated with the mixer circuit. However, such tuning will probably not be necessary since the expected 20 dB gain of the preamplifier and mixer reduce the noise contribution of the IF amplifier to less than 0.1 dB at its present performance level.

2.2 RF Preamplifier

A schematic diagram of the preamplifier is given in Fig. 2.8. This design uses a 300 μm wide GaAs FET with a 1 μm long gate. It is expected to provide ~8 dB gain over the 7.75-8.25 GHz band as shown in Fig. 2.9. This

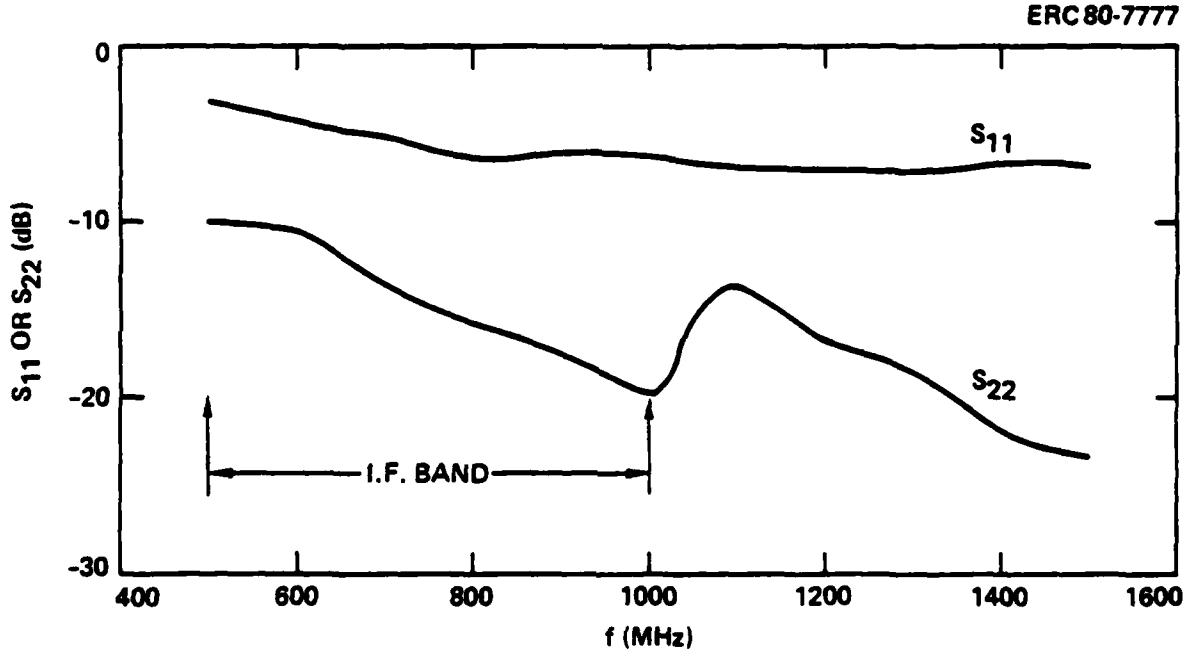


Fig. 2.7 Measured S_{11} and S_{22} of IF amplifier.

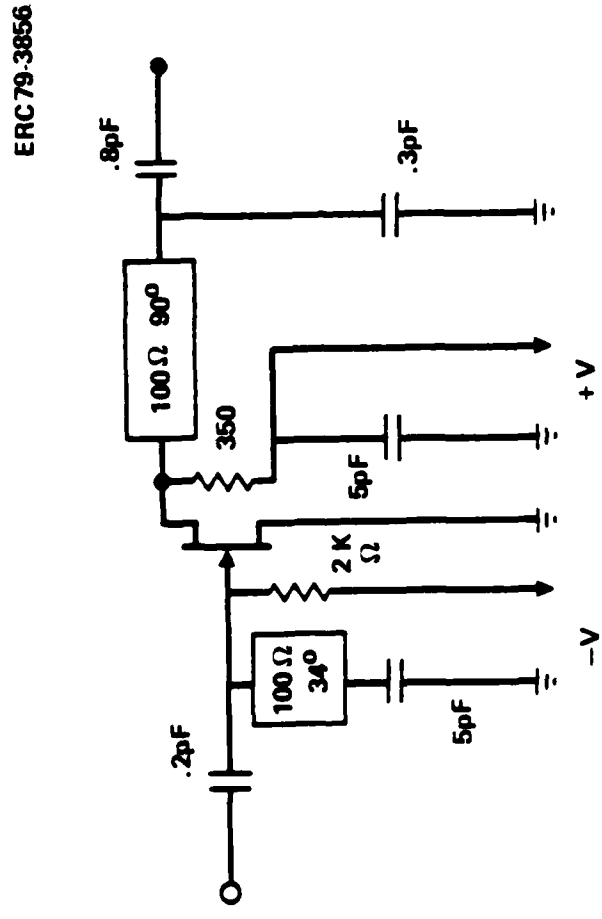


Fig. 2.8 Circuit diagram of 8 GHz RF preamplifier.

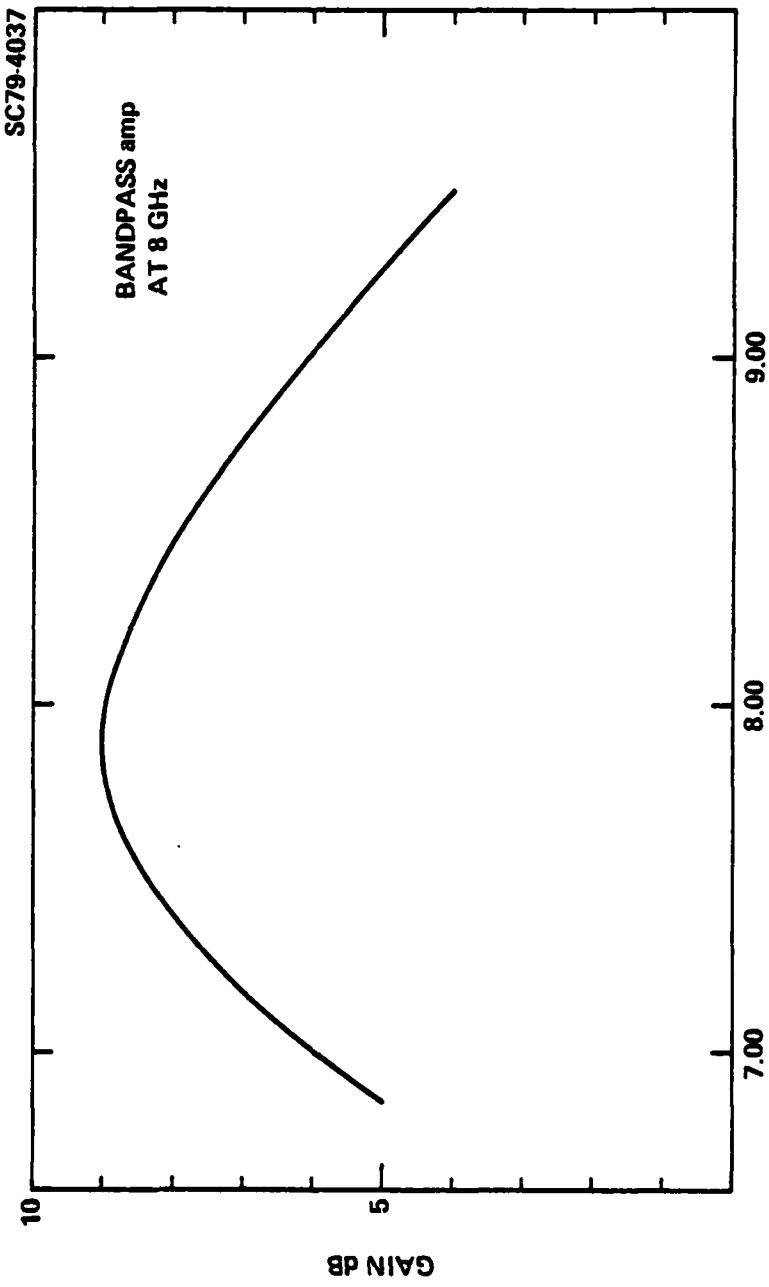


Fig. 2.9 Gain of a single stage RF preamplifier designed for a 7.75 to 8.25 GHz band.

performance curve was obtained by modeling the circuit of Fig. 2.8 on COMPACT CAD program. The noise figure of this amplifier is expected to be less than 2.3 dB at 8 GHz.

Figure 2.10 is an SEM photograph of an actual circuit. As for the IF amplifier, microstrip circuitry on a 635 μm thick semi-insulating GaAs substrate is the transmission mode used. RF grounding of the device source terminal is achieved by top surface ground planes. All bias points are bypassed on the chip by 5 pF MIM capacitors. Both interdigital and MIM capacitors are used for tuning purposes. RF performance of this circuit is being characterized at present and the results will be presented in the next report. A sensitivity analysis has been performed on this amplifier. The results are presented in the following section.

2.2.1 Sensitivity Analysis of the 8 GHz Amplifier

Sensitivity analysis is a vital part of the MMIC design process to achieve device performance similar to the predicted response. Slight process variations will cause all circuit parameters to vary from wafer to wafer, and the active devices will be especially sensitive to these process variations. Narrow band amplifier circuits are most vulnerable to element value perturbation for two reasons. First, they usually contain high Q circuits which are easily frequency skewed or de-tuned from adjoining resonant circuits. Second, as the narrow band input and output circuits are tuned to different center frequencies gain falls off rapidly. Often the circuit design must be modified to avoid extreme element sensitivity, even at the expense of a slight degradation in performance. Unlike other technologies, circuit tuning after fabrication is impractical in the MMIC approach.

Figure 2.11 shows a model of the 8 GHz amplifier and Table 2.1 shows the effect of a ±10% change in the key element values. In Figure 2.11, R_g and R_d are required for stabilization and their values are not critical. C_{in} and C_{out} are tuning elements as well as DC blocking capacitors. Cp and Lp form a resonant circuit for some tuning and Lp is also used for bias insertion. The major tuning elements in the circuit are T_1 which resonates with the internal

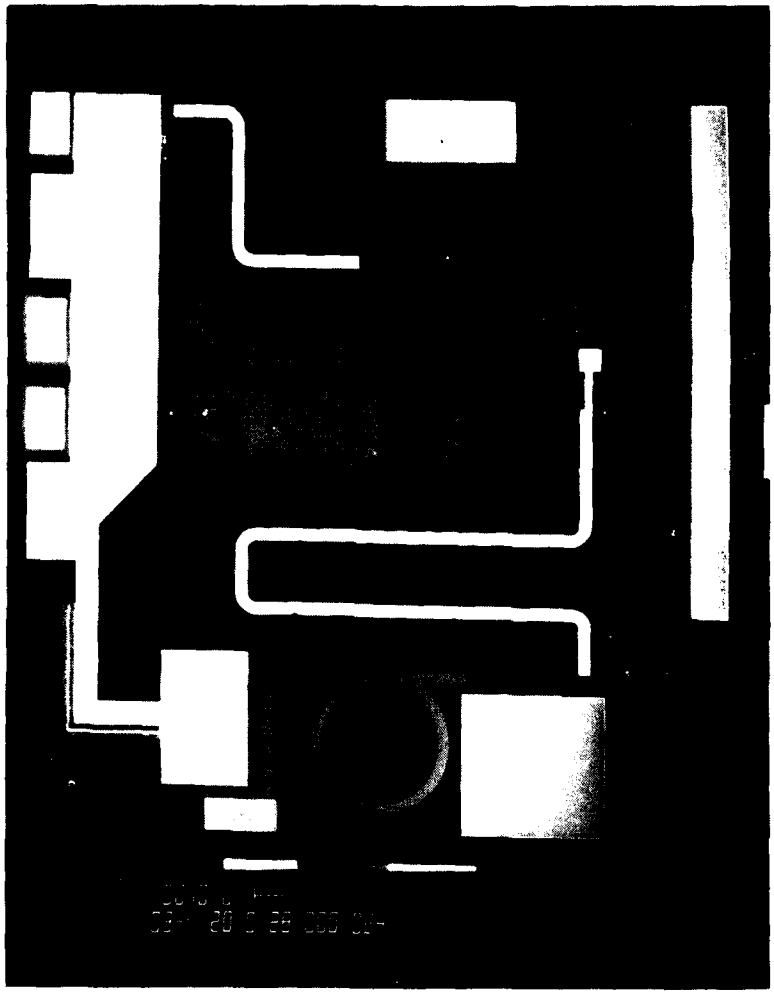


Fig. 2.10 SEM photograph of 8 GHz preamplifier chip. Chip size is 2.5 x 2.5 mm^2.

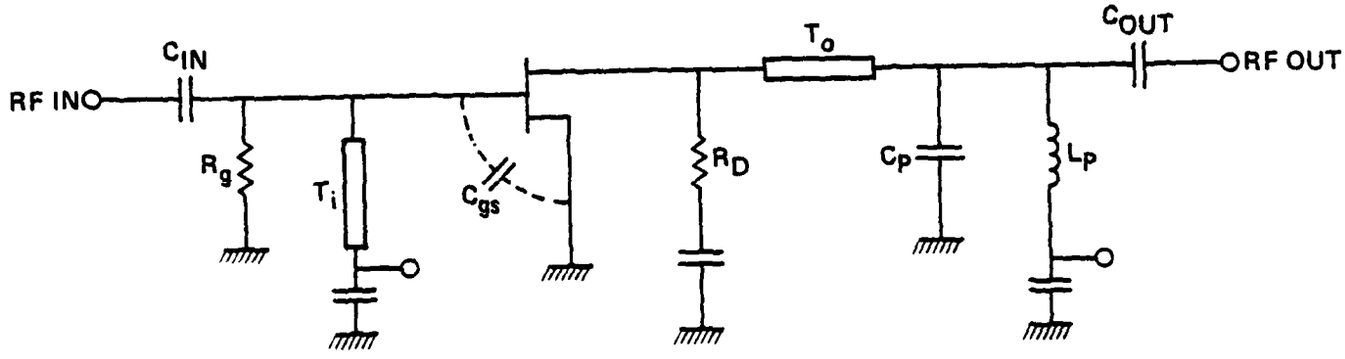


Fig. 2.11 Amplifier circuit for sensitivity analysis.

gate capacitance of the FET, C_{gs}, and T_o. Since C_{gs} and T_i are resonant, an increase in either C_{gs} or the effective length of T_i will produce a lower operating frequency. Note that the sensitivity to changes in T_i is larger than the sensitivity to changes in C_{gs}. This is a common effect when distributed elements are used in LC resonant circuits, since the tangent function has a slope larger than unity for moderately long lines. The output transmission line is mostly used for impedance transformation and small perturbations produce small variations in circuit response.

Although performance variations of any type are undesirable, changes which reduce the gain are preferable to those that cause pronounced variations in the frequency of operation. Low gain will degrade receiver performance, but a mistuned amplifier is useless on a monolithic receiver tuned to the original frequency. Parasitic elements were not considered in this analysis; however in the final layout they almost always reduce the frequency of operation. All circuit parameters must be re-optimized after the initial layout and its associated parasitics are known. Several iterations will often be required.

Table 2.1
Gain vs Frequency for a 10% Change in Element Values

	Frequency (GHz)							
	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5
Nominal	-1.19	2.09	5.50	8.39	9.26	8.12	6.44	4.86
T_i + 10%	0.92	4.56	8.01	9.63	8.64	6.84	5.18	3.76
T_i - 10%	-3.29	-0.33	2.79	5.88	8.25	8.77	7.69	6.13
C_{gs} + 10%	-0.84	2.58	6.09	8.76	9.00	7.49	5.76	4.21
C_{gs} - 10%	-1.54	1.62	4.91	7.89	9.33	8.66	7.10	5.53
T_o + 10%	-1.01	2.32	5.75	8.53	9.18	7.90	6.15	4.51
T_o - 10%	-1.37	1.85	5.21	8.13	9.18	8.19	6.60	5.10

2.3 Dual Gate FET Mixer

A circuit diagram of the dual gate FET mixer is shown in Fig. 2.12. This design incorporates a 500 μm wide dual gate FET for mixing and a 300 μm wide FET at the IF output port. The gain of this circuit measured from the signal gate to the output is of a low pass nature, giving +15 dB of gain at 1 GHz, and -7 dB at 8 GHz. The output transistor is connected in the source follower configuration. The high input impedance of this stage is a necessary component of the low pass nature of the drain circuit of the dual gate FET. It also provides a 50 Ω output impedance at the IF frequency. Figure 2.13 is an SEM photograph of an actual circuit. This circuit also uses a 635 μm thick GaAs substrate, microstrip transmission lines, and a top surface ground plane for grounding of active and passive elements. All bias lines are bypassed with integral MIM capacitors of ≳5 pF value. RF performance of this circuit is being characterized at present. The results will be presented in a later report.

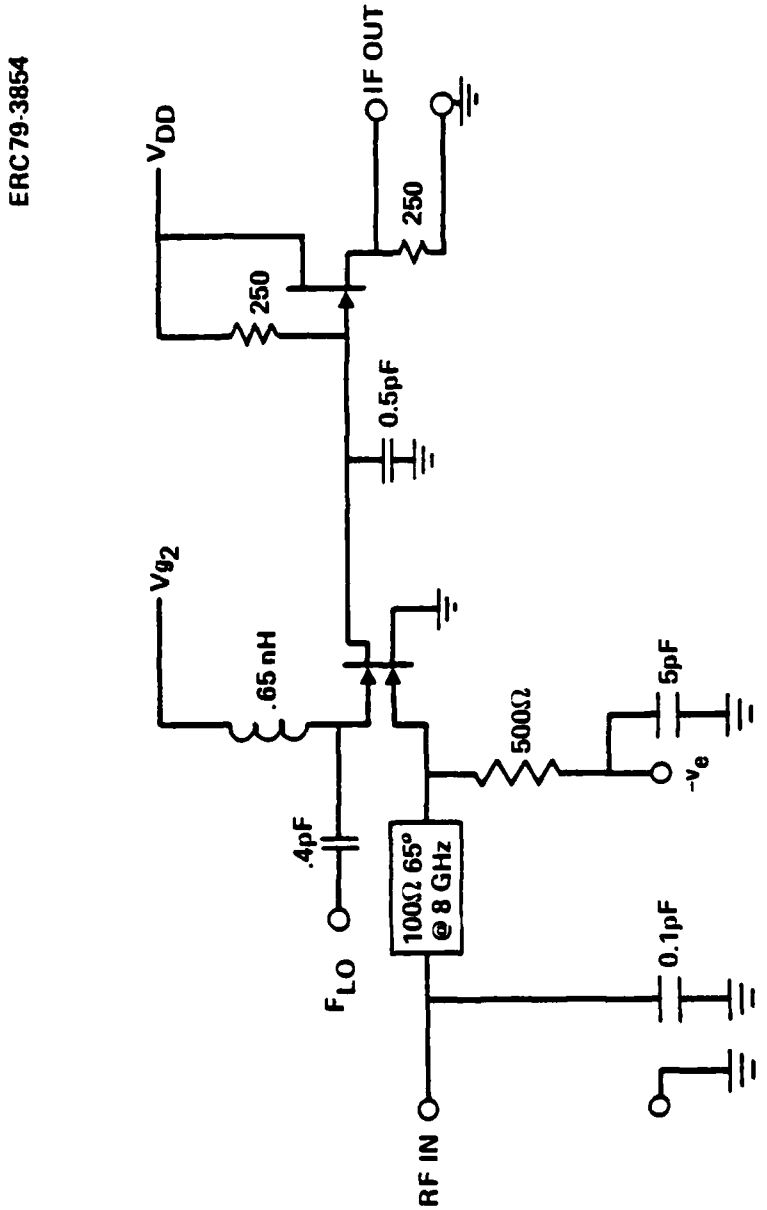


Fig. 2.12 Circuit diagram of 8 GHz dual gate FET mixer.

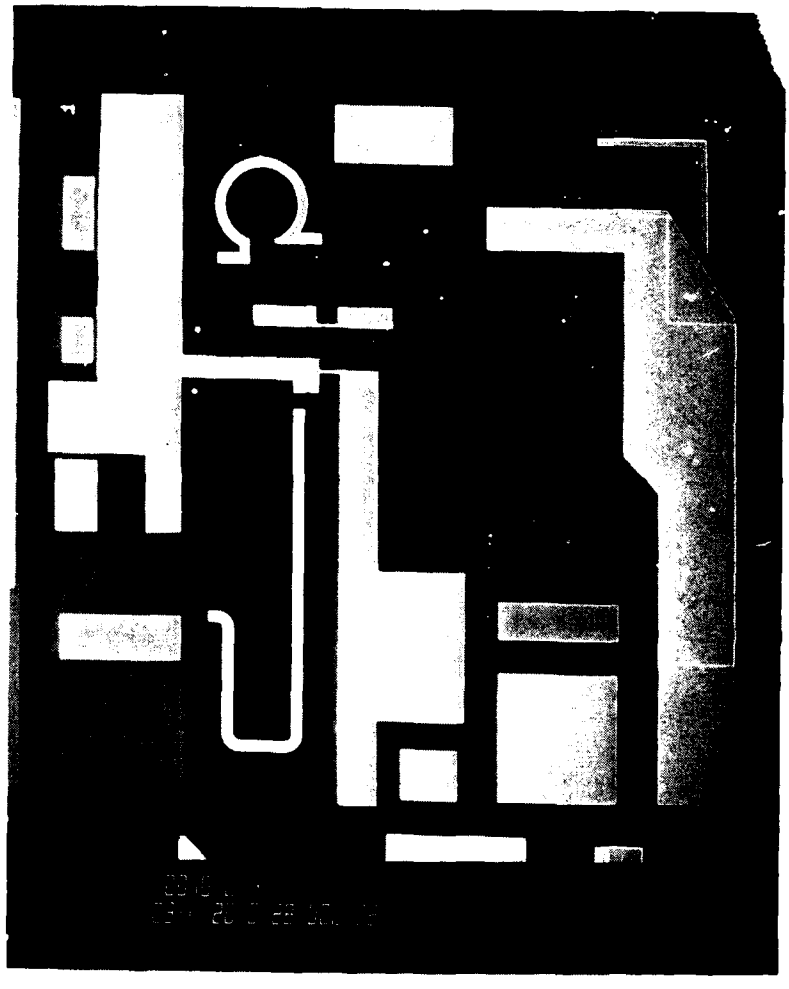


Fig. 2.13 SEM photograph of the 8 GHz dual gate FET mixer. Chip size is approximately 2.5 x 2.5 mm^2.

CHAPTER 3

Circuit Fabrication Technology

The circuits described in this report have been fabricated on semi-insulating gallium arsenide substrates using state-of-the-art high yield processes. Complex monolithic microwave integrated circuits (MMICs) require more than one type of device (FETs, varactor diodes, etc.) for their operation and the optimization of the performance of each device may require more than one type of active layer on the same substrate. To accommodate this need, the fabrication techniques implemented in the MMIC program are based on multiple, localized ion implanted active layers leading to highly reliable planar structures. The mesa approach is also used in those cases where only one type of active layer is required. It has the advantage of increased throughput due to reduced turnaround times.

Direct, localized ion implantation in semi-insulating GaAs for active layer formation has made it possible to conceive of fabrication schemes not possible under the limitations of epitaxial growth or implantation over the full wafer. Localized implantation provides automatic isolation between devices. The advantages of uniformity, reproducibility, versatility, and low cost of this technique are difficult to match by other material technologies.

A cross-sectional view of a typical MMIC is shown in Fig. 3.1. In addition to the elements shown there, it is necessary to provide ground points, DC bias points, and RF connections. Typical components required are capacitors, resistors, transmission lines, FETs, varactor diodes, and level shifting diodes. A two-level metallization scheme is used with plasma deposited silicon nitride as the crossover insulator and the dielectric for metal-insulator-metal capacitors. Capacitors can be either interdigital or metal-insulator-metal depending on the value required. Interdigital capacitors are defined in the first level metal by contact photolithography for high resolution and reproducibility. Only low values of capacitance are realizable in this form since for large values a large chip area is required which also produces a large parasitic capacitance to ground. For large values of

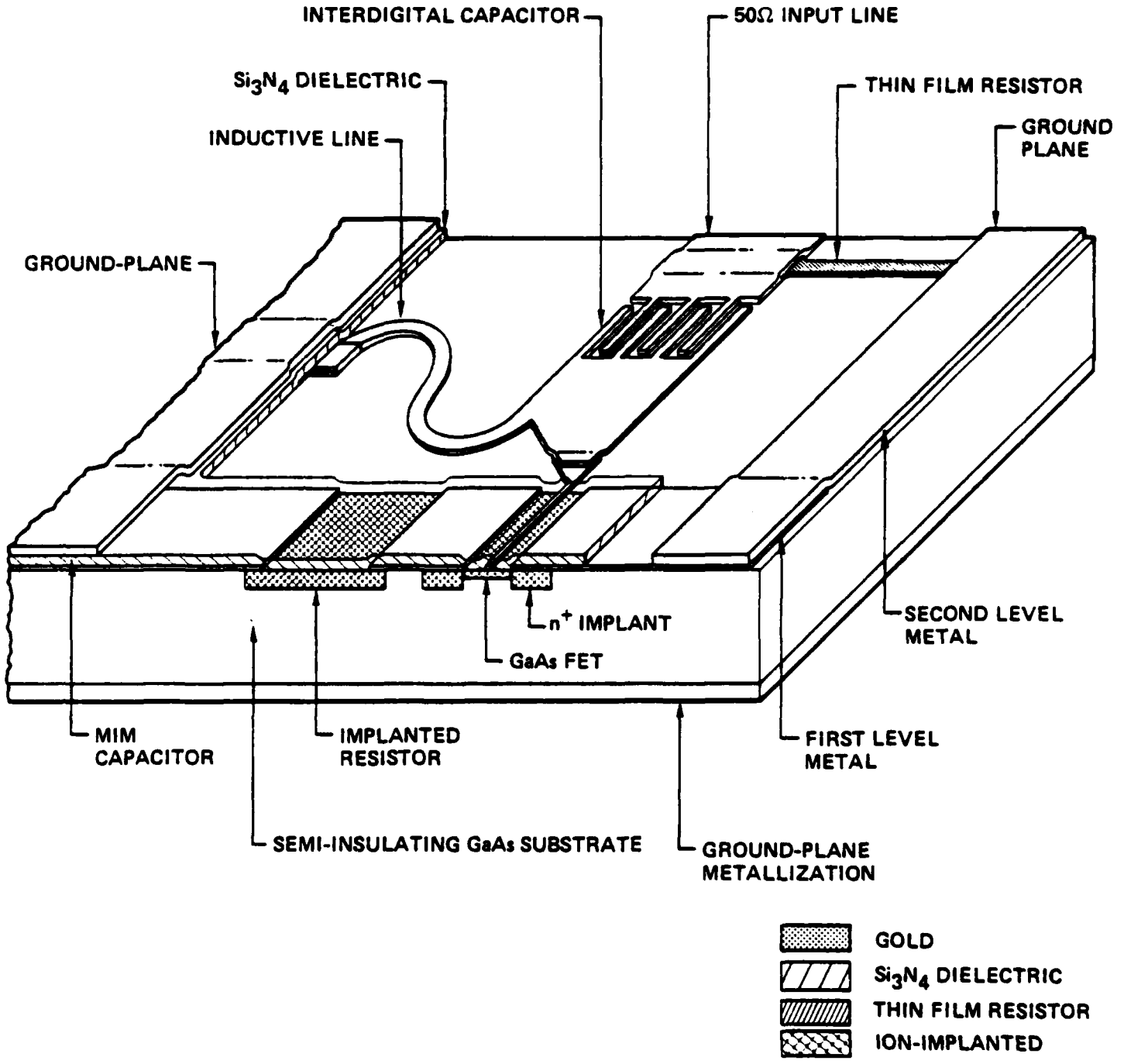


Fig. 3.1 Schematic diagram of a monolithic microwave integrated circuit.

capacitance, metal-insulator-metal capacitors are perferred. Capacitances up to 125 pF/mm^2 are presently attainable with these capacitors.

Resistors are fabricated as either ion implanted or thin film metal resistors. Thin film resistors have a large linear region but require an additional mask level. For very large values of incremental resistance, self biased FETs or saturated ion implanted resistors can be used.

Transmission lines are usually constructed in the form of microstrip. Although co-planar and slot line techniques can be used, they consume large chip areas and can cause some interconnection problems. Via holes and edge of chip wraparounds are used for grounding in the case of microstrip transmission lines.

RF connectors are provided as 50 ohm transmission lines that run to the edge of the chip. DC connections are bonding pads and their associated metal-insulator-metal bypass capacitors.

Fabrication of the structure described above requires sophisticated techniques. Both substrate selection and the fabrication process have to be carefully controlled. These topics are addressed in Sections 3.1 and 3.2, respectively.

3.1 Ingot Qualification

The fabrication of MMICs begins with the qualification of the semi-insulating substrate to assess its ability to withstand high temperautre (850°C) processing. The compensating impurities and defects in the substrate must not affect the electrical properties of the ion implanted layer, so that carrier concentration, mobility, carrier lifetimes, etc., depend only on the identity and dose of the implanted ions. Meeting this condition would ensure that the electrical properties of the implanted layers are independent of the substrate and will aid uniformity and reproducibility. In addition, unimplanted portions of the semi-insulating substrate must retain their high resistivity after a wafer has been capped and annealed to remove damage in the implanted portions, so that electrical isolation is maintained between the doped regions. The pre-selection tests for bulk semi-insulating GaAs

substrates involve qualification of the entire ingot by sampling the front and the rear of each boule. Extensive data has dhown that all wafers within the ingot are qualified when samples from both ends pass the qualification tests. The electrical criteria for qualification involve the following two tests:

(1) Thermal Anneal: The semi-insulating wafer is capped with sputtered Si_3N_4 and annealed at 850°C for 30 min in a H_2 ambient. A sheet resistance $>10^7$ Ω/□ must be maintained following the anneal.

(2) Selenium Implantation: The wafer is implanted with 3×10^{12} cm^{-2}, 300 keV Se ions at 200°C. It is then capped and annealed as in 1. The resultant test pieces are subjected to C-V and Hall measurements to characterize the active layer and verify that it is suitable for device fabrication. Typical doping profiles in Cr doped and undoped semi-insulating substrates are as shown in Fig. 3.2.

By following these qualification tests, excellent reproducibility and uniformity of device parameters is achieved. This is shown in Tables 3.1 and 3.2 which list the variation in pinch-off voltage, V_p and the transconductance, g_m of 300 μm, Se implanted GaAs FETs from 5 different wafers.

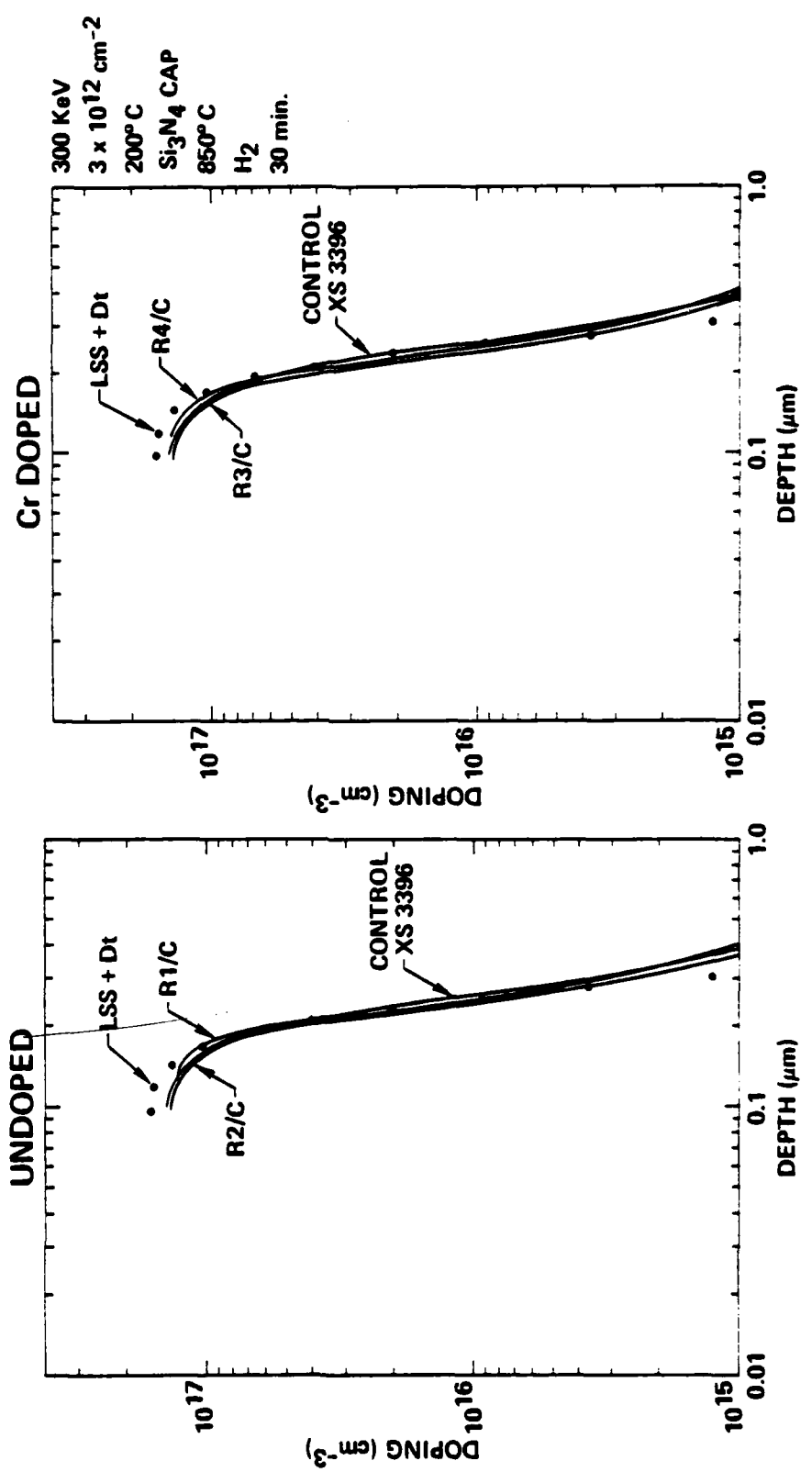


Fig. 3.2 Doping profiles obtained by Se ion implantation in semi-insulating GaAs.

Table 3.1

Transconductance of Selenium Implanted GaAs FETs

Wafer	Transconductance of Selenium Implanted GaAs FETs Mean g_m (mS)	σ (mS)	Depletion Voltage of Se Ion Implanted GaAs FETs Mean V_p(V)	σ(V)
F31	21.2	2.3	2.54	0.38
F32	23.1	1.4	2.05	0.28
F33	21.1	1.8	3.11	0.21
F34	23.6	3.1	2.45	0.28
F37	24.6	2.0	2.61	0.20
Avg.	22.8	1.9 (±8%) Avg.	2.75	0.31 (±11%)

Table 3.2

Summary of Wafer Uniformity and Reproducibility By Ion Implantation

Wafer Properties	Ion Implantation
Active layer uniformity (V_p)	±7.8%
Reproducibility (V_p)	±11%
Buffer layer capability	none
n^+ capability	10^{18} Si
Planar capability	yes

3.2 Circuit Fabrication Steps

The circuits described in this report were fabricated on 635 μm thick semi-insulating GaAs substrates using microstrip transmission line circuitry. Top surface ground planes are provided near the chip edges to allow low parasitic inductance grounding of active and passive devices.

A Se implant of 1000 Ω/□ is used for device active layers and resistors. Both interdigital and metal-insulator-metal (MIM) capacitors are used for tuning and RF bypassing purposes. Contact photolithography is used for all the steps including definition of the 1 μm long gates of FETs. The mask set has seven levels as described below:

Level	Function
1	Mesa/Active Layer
2	Ohmic Contact
3	Gate and First Level Metal
4	Via Hole
5	Second Level Metal
6	Fiducial Alignment Marks
7	N^+ Contact

All seven levels are needed if a planar circuit with n^+ contacts is to be fabricated. If however, a mesa approach without n^+ contacts is desired, only the first 5 mask levels need be used. Details of the important fabrication steps are given next.

(1) Active layer implant: Se, 300 keV, 3.0×10^{12} cm^{-2} at 200°C substrate temperature. A peak doping of $\sim 1.5 \times 10^{17}$ cm^{-3} and a pinch-off voltage of ~3.5 volts is obtained (see Fig. 3.2). Definition of active areas may be accomplished by either mesa etching or by selective implantation using a photoresist

mask. Fiducial alignment marks are defined on the wafer surface for subsequent realignment capability when selective implantation is used.

(2) Cap and anneal: 1100A of reactively sputtered silicon nitride is used as a cap. Annealing is done at 850°C for 30 min in hydrogen.

(3) Define mesas (as necessary): This step is required only if the implantation is made over the entire wafer. Although this results in a nonplanar structure, it is often used to reduce the turnaround time. 3000A high mesas are defined using a chemical etch.

(4) Form ohmic contacts Eutectic Au Ge and Pt are evaporated using an electron beam source. The contacts are alloyed at 450°C for 1 minute in forming gas.

(5) Deposit plasma silicon nitride.

(6) Deposit Gate and First Level Metal (Ti/Pt/Au): The importance of being able to reliably define the gate electrode of FETs cannot be overemphasized. In order to minimize the parasitic gate resistance, the thickness of the gate metal must be made as large as practical. The yield of the gate definition step,

however, decreases rapidly with increasing metal thickness when conventional lifting techniques are used in conjunction with photoresist. In order to increase the lifting capability of photoresist the process shown in Fig. 3.3 has been developed. A layer of silicon nitride is deposited on the GaAs and the gate pattern is defined in the photoresist. The exposed nitride is then etched in a plasma. Due to the increased distance between the top of the resist and the surface of the GaAs, thicker metallization may be deposited and lifted. Figure 3.4 shows two 1 μm long gates, spaced by ~1 μm, in a 6 μm gap between the source and the drain of a dual gate FET. Note the excellent edge definition obtained by this technique. Reactive ion etching was used in this case to minimize the undercutting in the nitride.

The first level metallization contains the interdigital capacitors, the bottom plates of MIM capacitors, ohmic contact overlays, and interconnecting lines. In attempting to define this by conventional lifting techniques, it was observed that the edges were ragged due to the tearing involved at these points. This is shown schematically in Fig. 3.5a. These sharp edges are not well covered by the subsequent step of dielectric deposition which forms the "I" layer of MIM capacitors. This results in a very poor yield of MIM capacitors made on wafers processes in this manner. The nitride aided lifting process

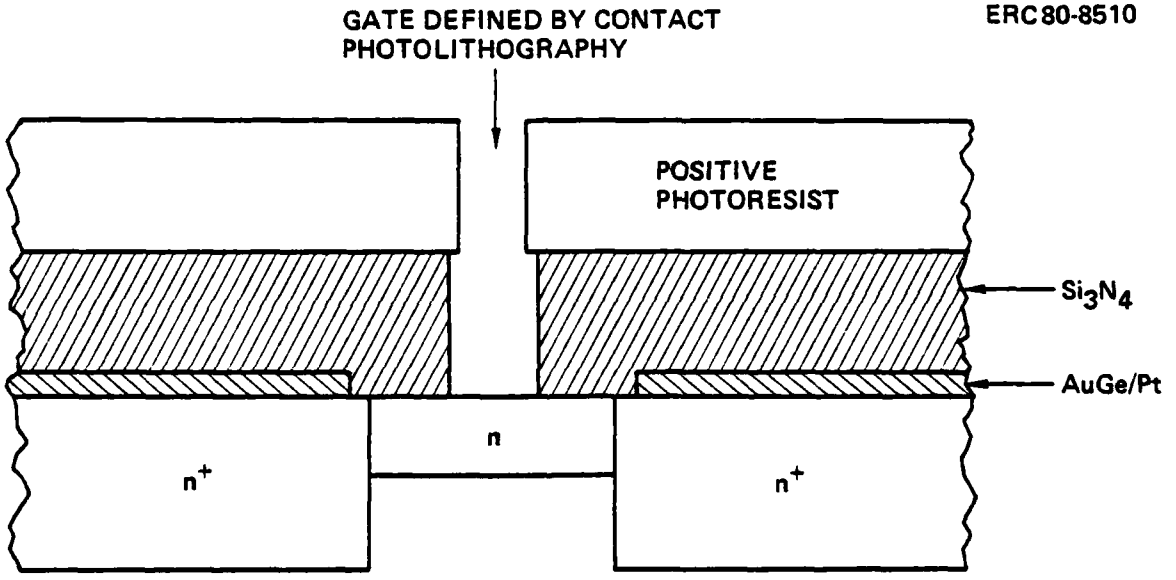


Fig. 3.3 A schematic diagram showing the nitride aided lifting process. Si_3N_4 is deposited on GaAs and the gate pattern is defined in positive photoresist on top. Exposed Si_3N_4 is etched in a plasma. Gate metal is then evaporated and lifted as usual.

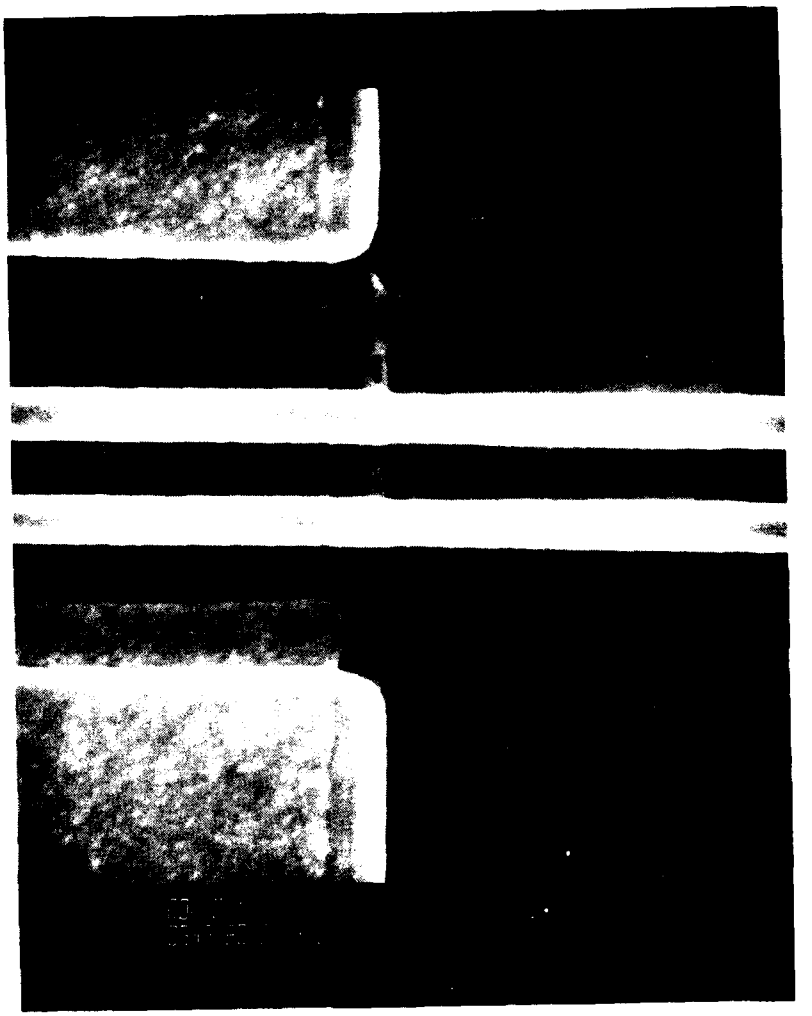
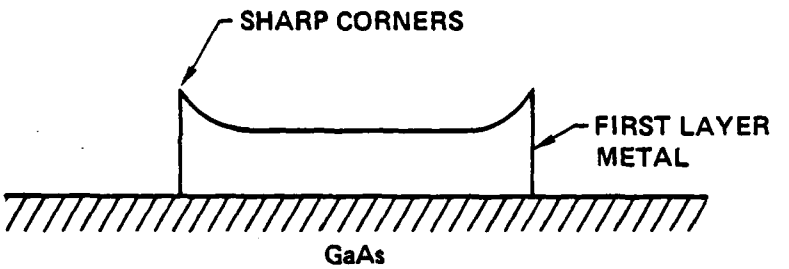
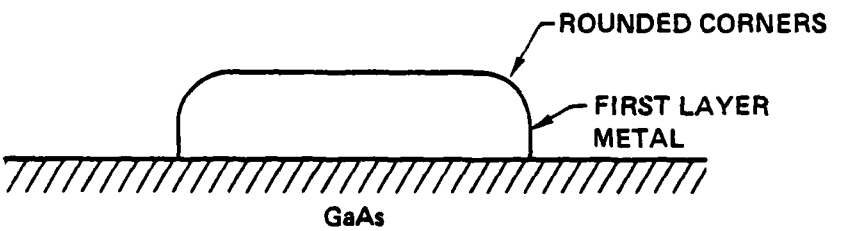


Fig. 3.4 Photograph showing the excellent edge definition obtained with nitride aided lifting. The two gates (~ 1 μm long) are spaced 1 μm apart in a 6 μm source-drain gap. Metal thickness is 5000Å.



(a)



(b)

Fig. 3.5 (a) Sharp corners obtained in defining thick gold patterns by the conventional lifting technique. (b) Smooth edges obtained by the nitride aided lifting technique.

eliminates the metal tearing providing metal thickness is less than the nitride thickness. This results in smooth edges (Fig. 3.5b) and a high yield of MIM capacitors.

(7) Deposit plasma silicon nitride: This nitride layer is used as the dielectric for the MIM capacitors and as the insulator for crossovers. It also provides a protection layer for the FETs.

(8) Open via holes: Via holes are opened in the silicon nitride layer wherever connections to the first level metal are desired. Standard photolithography and plasma etching is used for this purpose.

(9) Deposit second level metal: This metallization (Ti/Au) is used for the top electrode of MIM capacitors and all the inter-device matching circuitry. The gold is usually electroplated to a thickness of ~2-3 μm to reduce ohmic losses.

(10) Backside metallization.

(11) Saw wafer into individual chips.

A photograph showing all three circuits is given in Fig. 2.1. The RF preamplifier and the mixer are each 2.5 mm × 2.5 mm. The IF amplifier is 2 mm × 2 mm. A considerable portion of the chip area is allocated for the

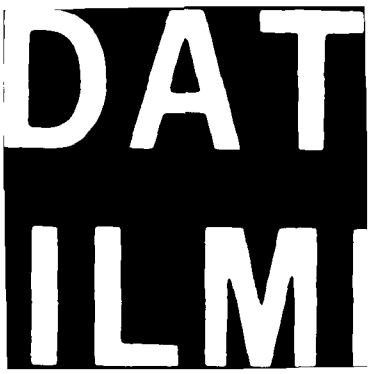
input/output bonding pads and the matching circuitry necessary to allow these circuits to be characterized in a 50 Ω system. The integrated chip, containing all three circuits, is expected to require a total chip area of 10-15 mm^2.

CHAPTER 4

Summary and Future Plans

This report has described the progress during the first phase of the development of a monolithically integrated superheterodyne receiver front end at 8 GHz. The components of the receiver (RF preamplifier, mixer, and IF amplifier) have been designed and fabricated on semi-insulating GaAs as functional monolithic circuits. Test results on the IF amp are 8.0 ± 1.5 dB gain from 500 to 1000 MHz and a noise figure of 6.2 dB across the IF band. Reduction of parasitic capacitances is expected to increase the gain by 2 dB and reduce the gain slope by 1 dB. The RF preamplifier and mixer chips are presently being characterized.

Second generation circuits will be designed at the completion of the characterization of the circuits described in this report. A new mask set will then be designed containing individual circuits and a preliminary integrated version of the receiver. The fabrication technology discussed in Chapter 3 will be upgraded as necessary, to improve circuit performance and yield.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